FIG_1

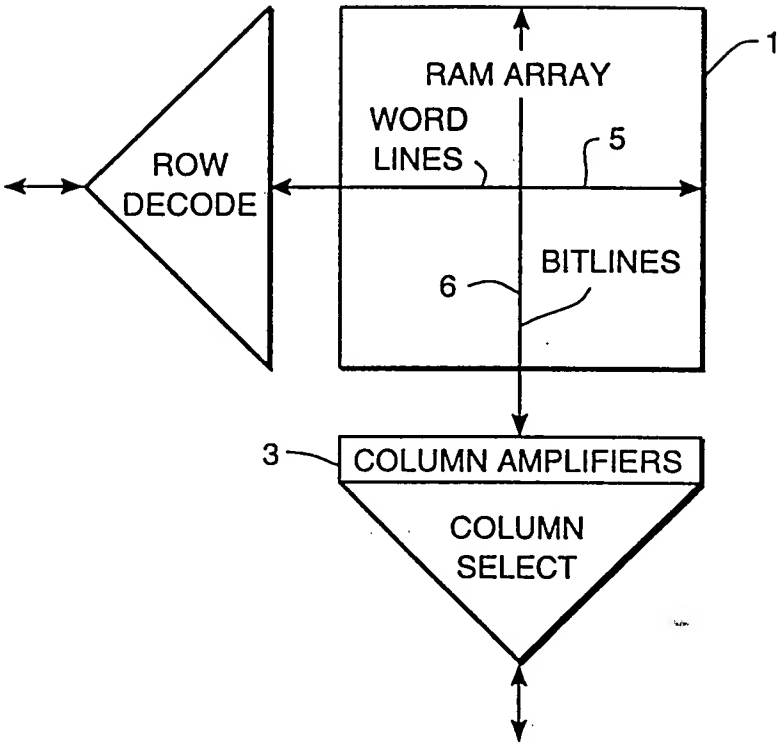

RAM ARRAY
1
WORD
LINES
5
ROW
DECODE
BITLINES
6
3
COLUMN AMPLIFIERS
COLUMN
SELECT

FIG_2

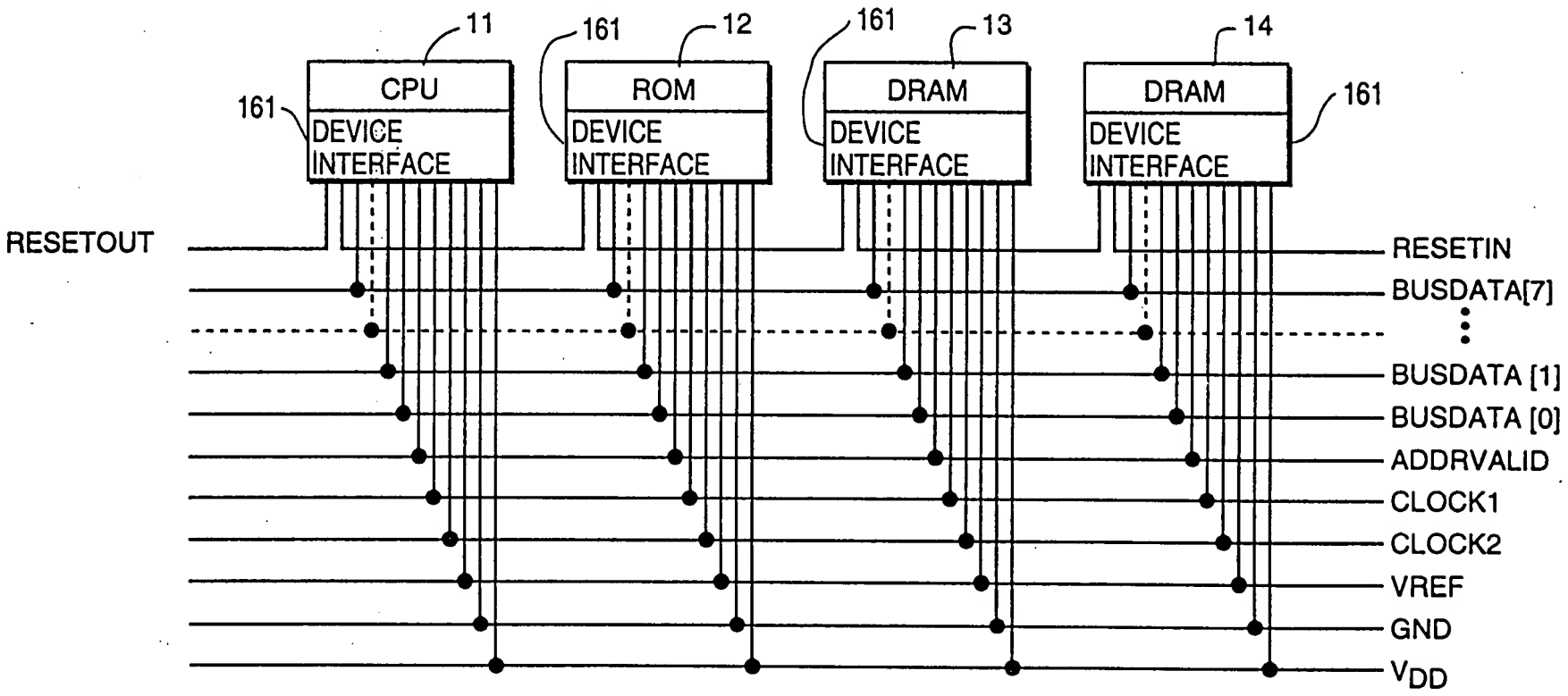
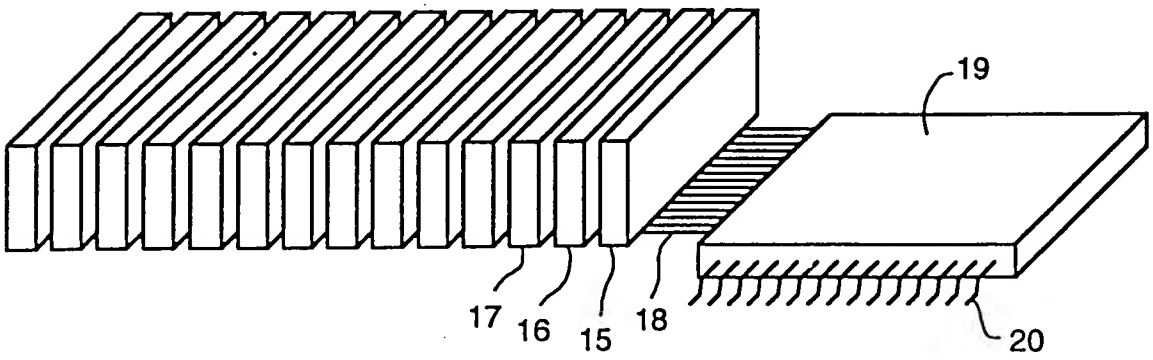

11
161
12
161
13
14
161
CPU
ROM
DRAM
DRAM
DEVICE INTERFACE
RESETOUT
RESETIN
BUSDATA[7]
BUSDATA [1]
BUSDATA [0]
ADDRVALID
CLOCK1
CLOCK2
VREF
GND
VDD

FIG_3



REGULAR ACCESS

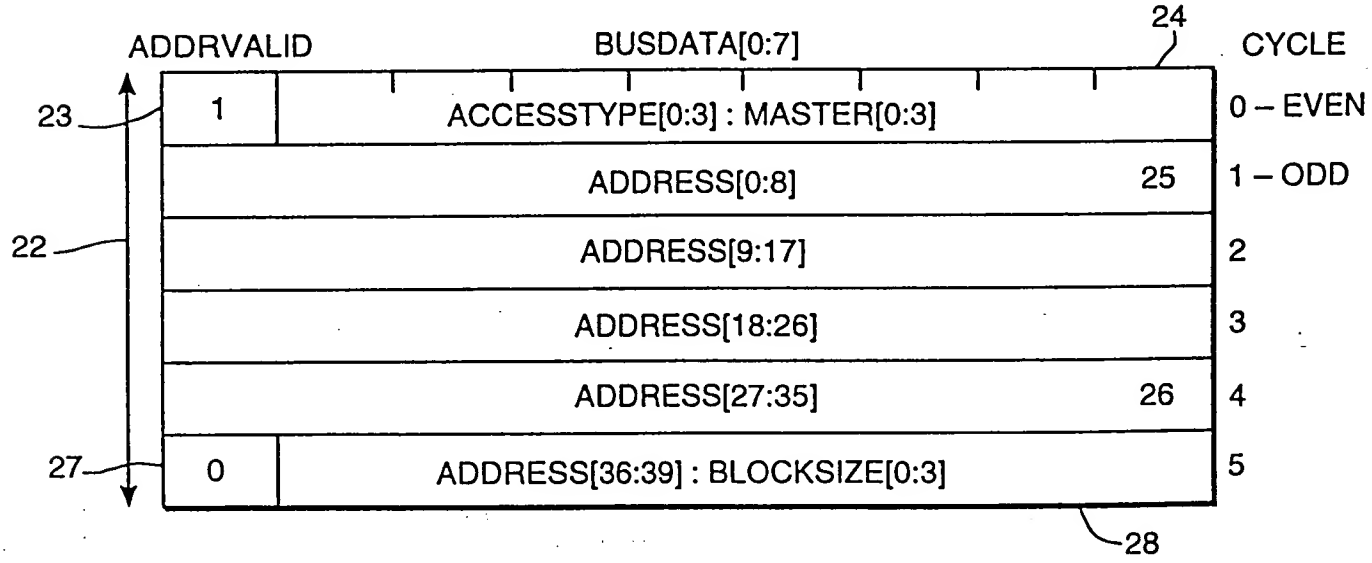


FIG_4

REJECT (NACK) CONTROL PACKET

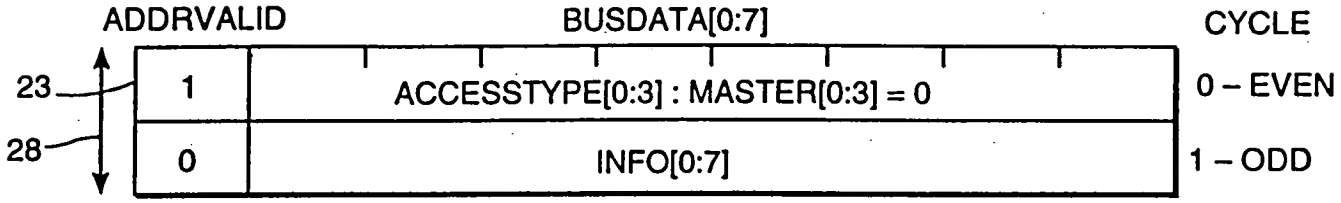


FIG_5

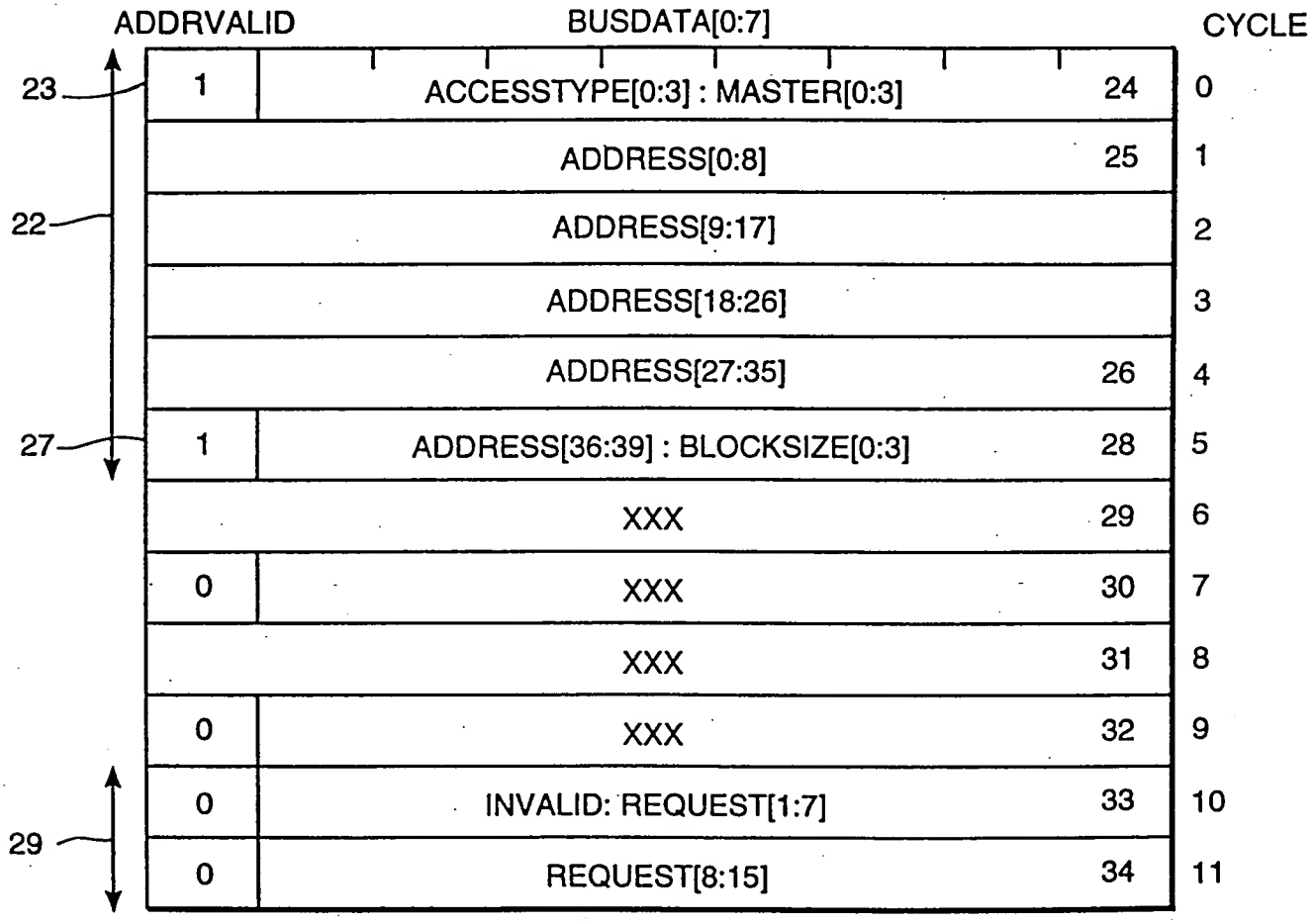


FIG_6

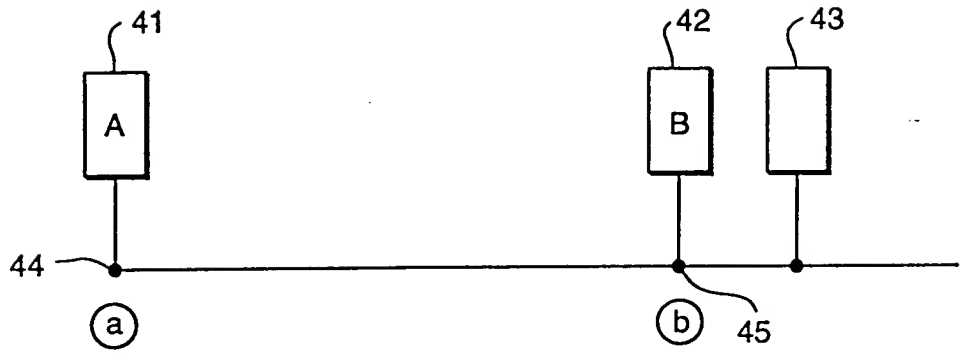


FIG_7A

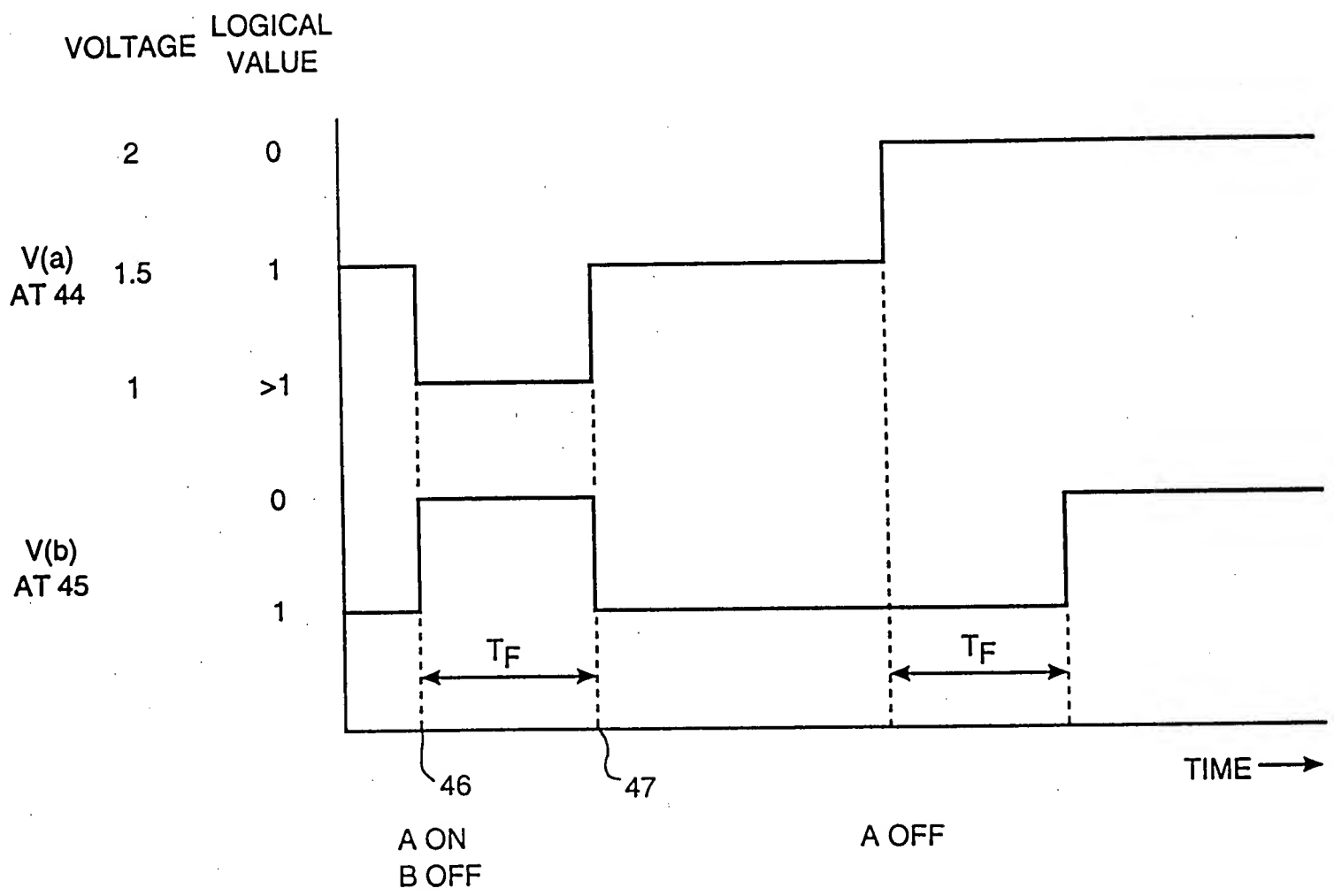

VOLTAGE
LOGICAL VALUE
2
0
V(a) AT 44
1.5
1
1
>1
0
V(b) AT 45
1
T_F
T_F
46
47
TIME
A ON
B OFF
A OFF

FIG_7B

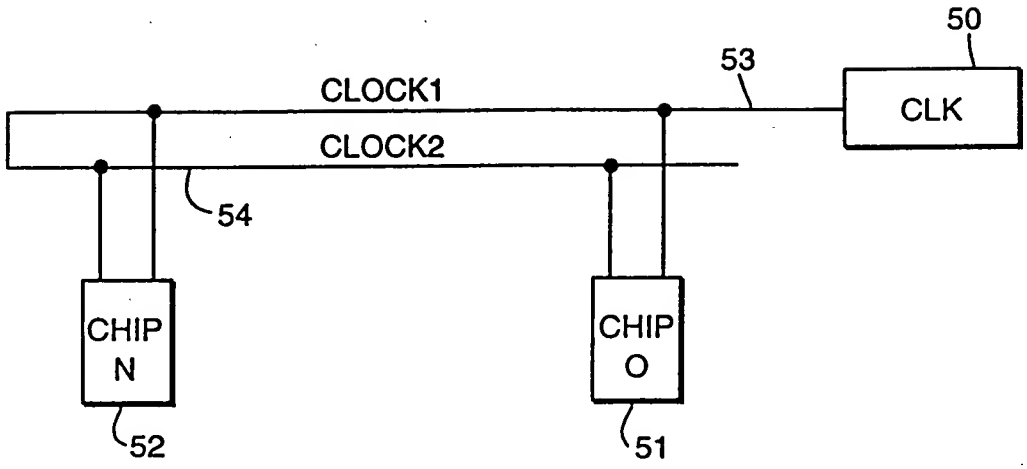

50
53
CLOCK1
CLK
CLOCK2
54
CHIP
N
CHIP
O
52
51

FIG_8A

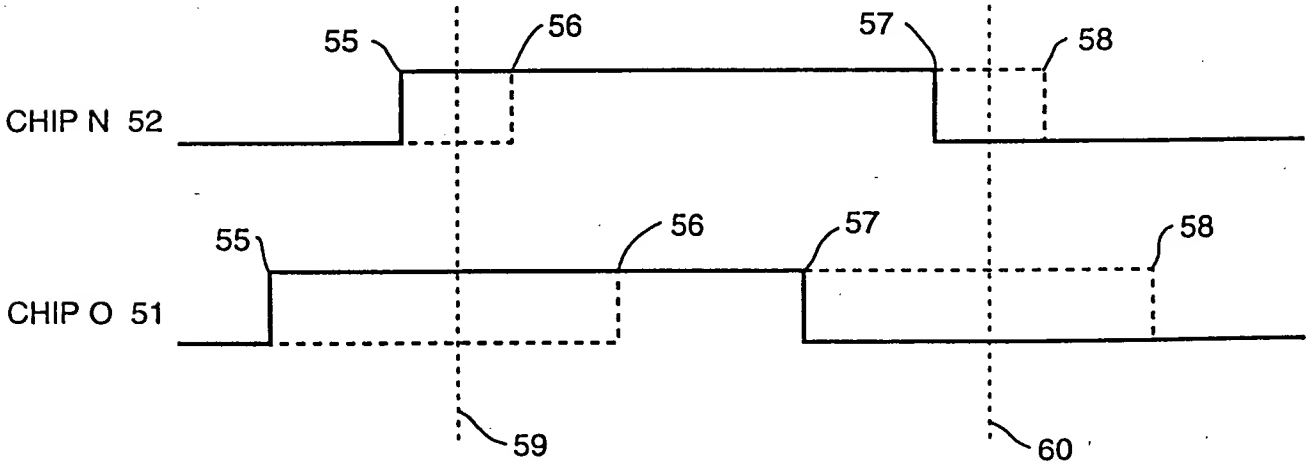

55
56
57
58
CHIP N 52
55
56
57
58
CHIP O 51
59
60

FIG_8B

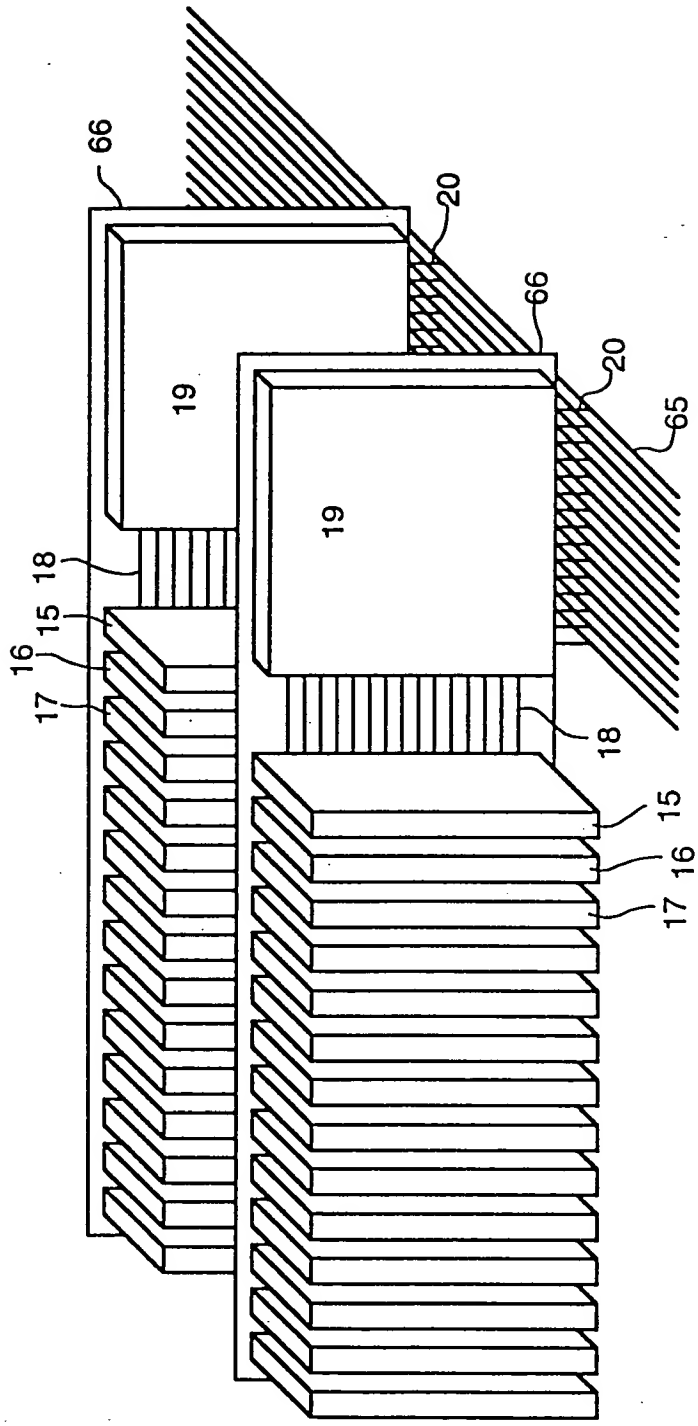


FIG_9

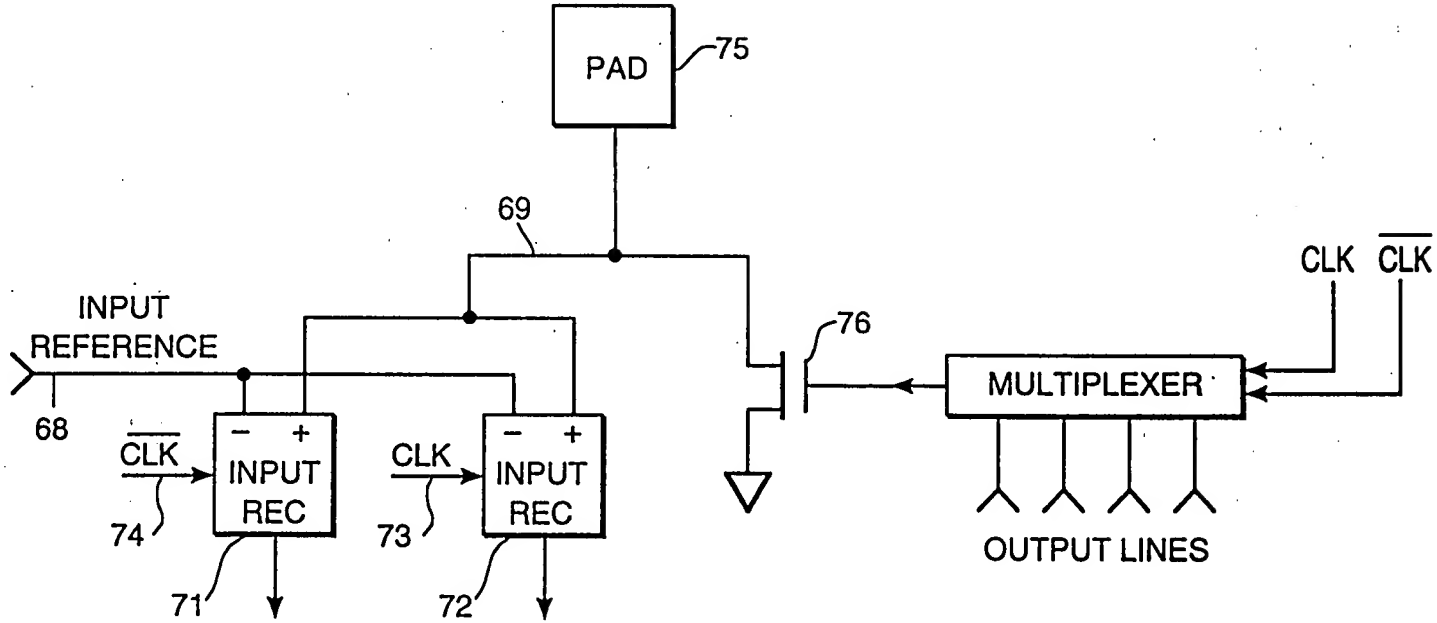

PAD
75
69
CLK
CLK
INPUT
REFERENCE
76
MULTIPLEXER
68
CLK
INPUT
REC
CLK
INPUT
REC
74
73
71
72
OUTPUT LINES

FIG_10

FIG_ 11

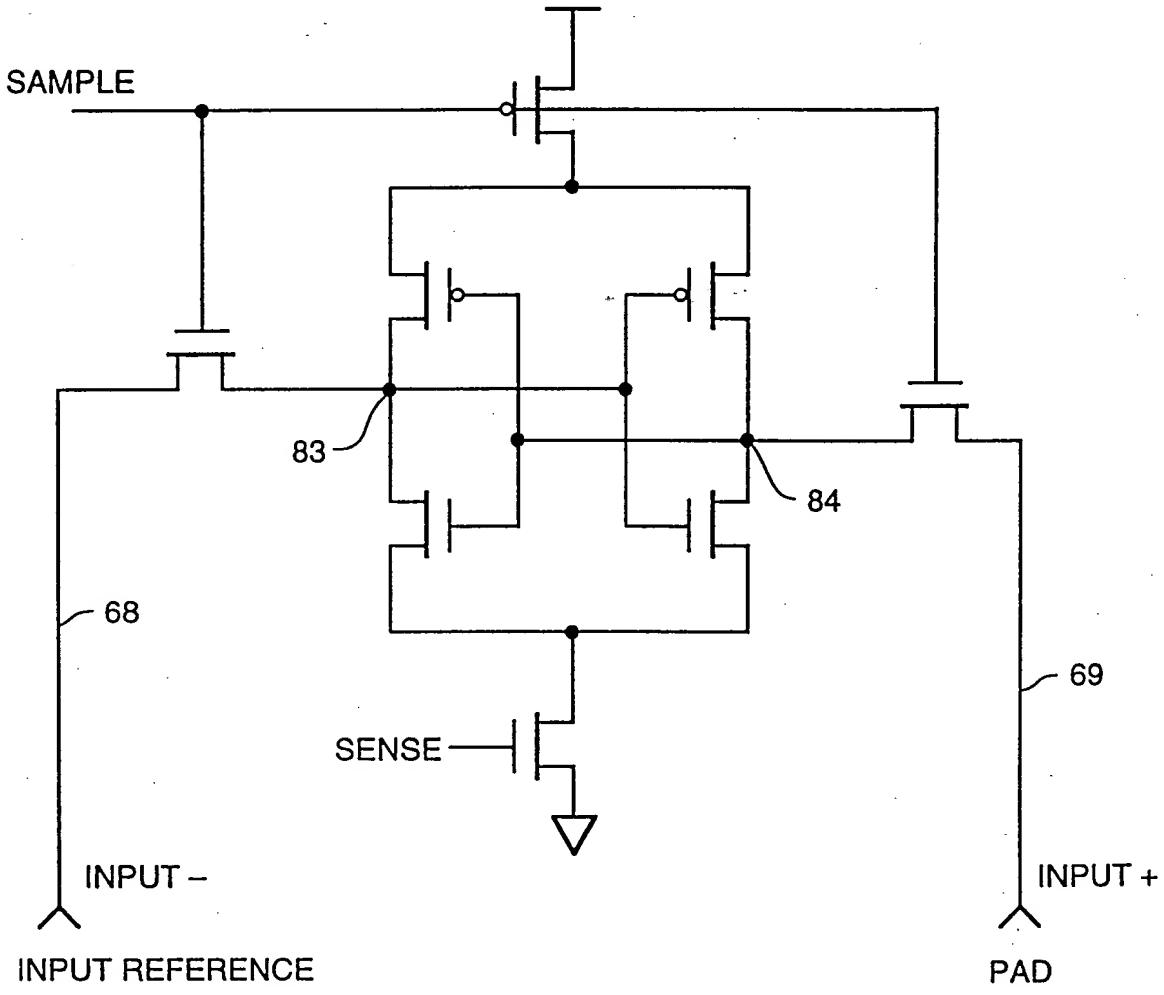


FIG_12

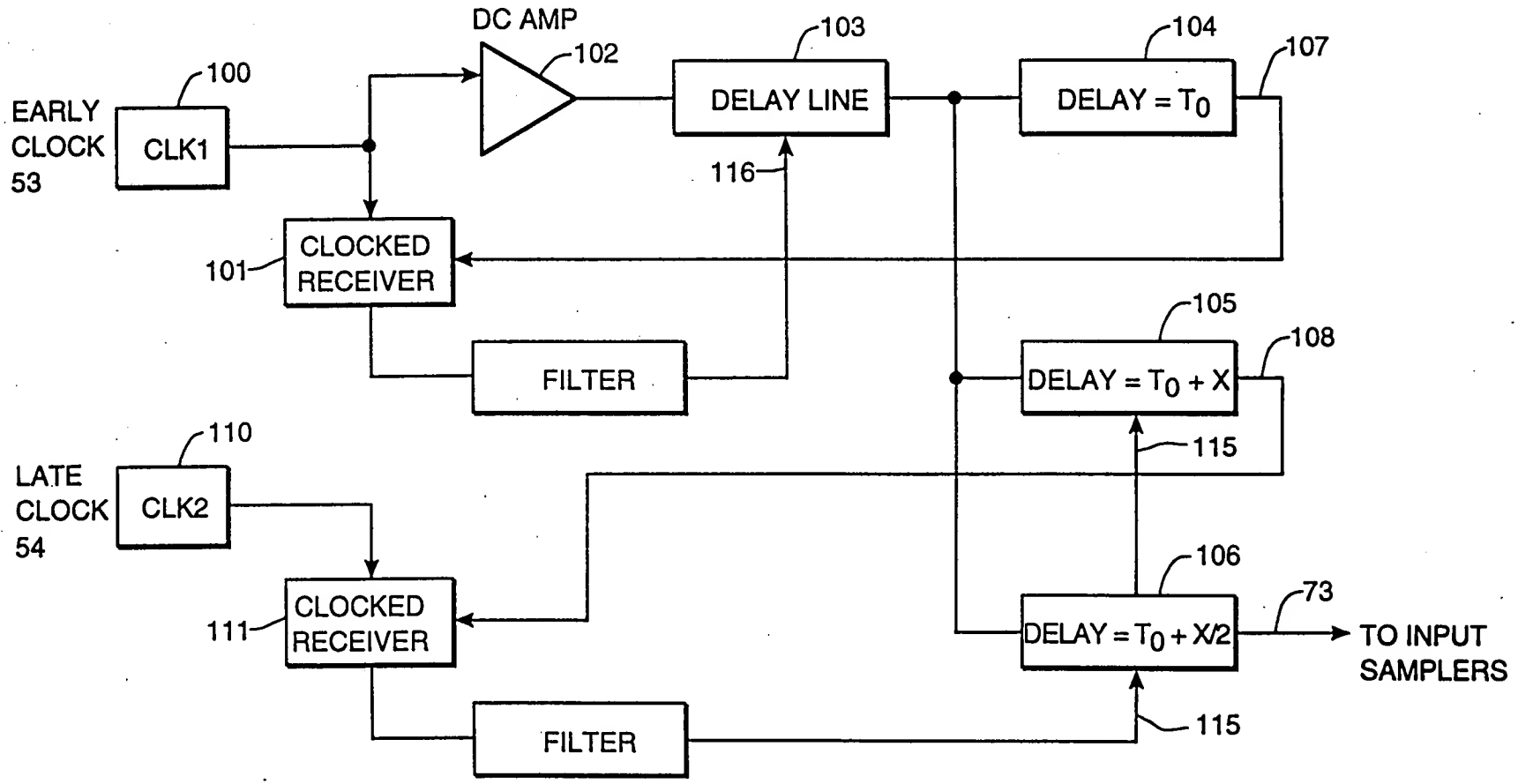
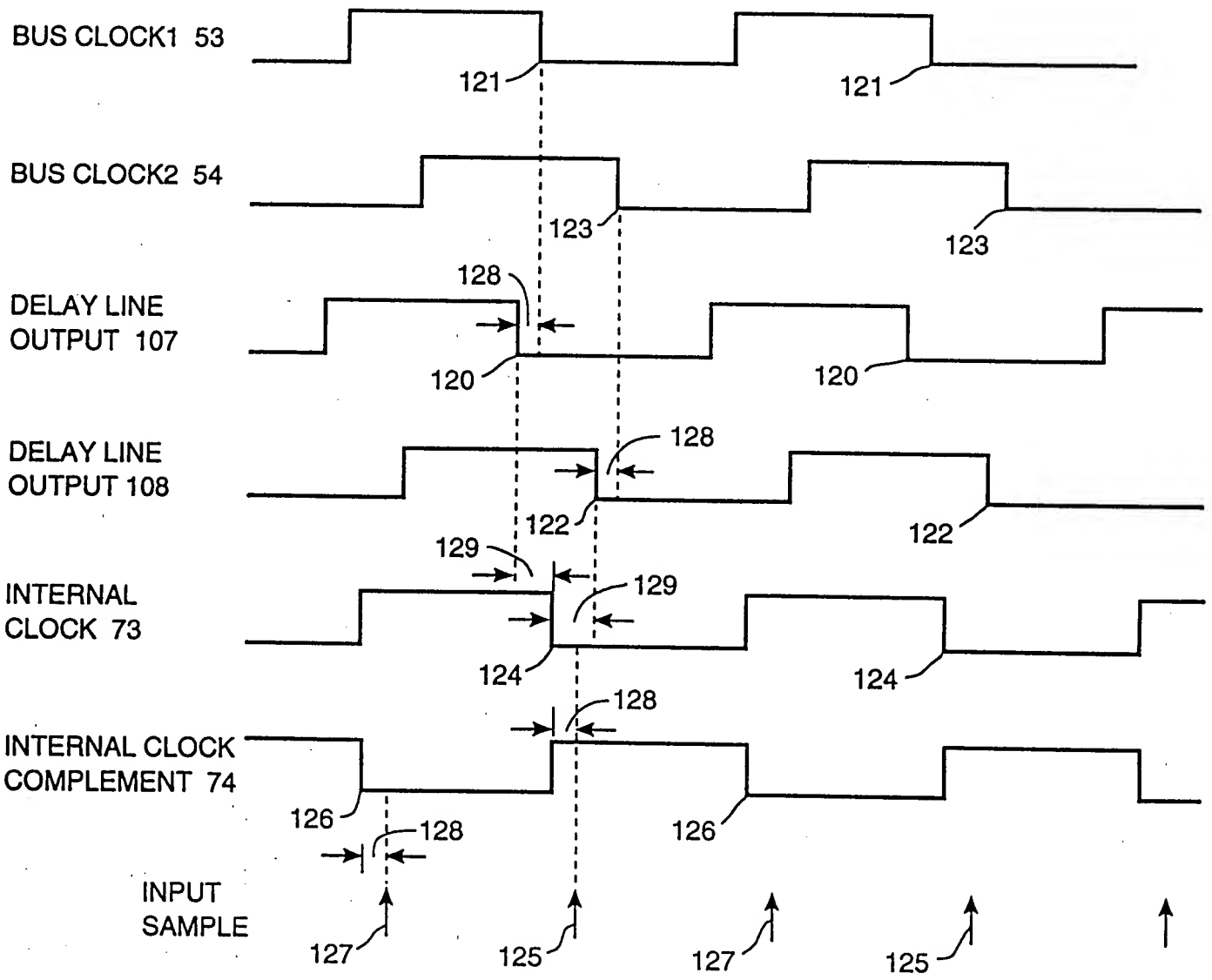

DC AMP
102
103
104
107
100
EARLY
CLOCK
53
CLK1
DELAY LINE
DELAY = T_0
116
101
CLOCKED
RECEIVER
105
108
FILTER
DELAY = T_0 + X
115
110
LATE
CLOCK
54
CLK2
106
73
CLOCKED
RECEIVER
111
DELAY = T_0 + X/2
TO INPUT
SAMPLERS
FILTER
115

FIG_13


BUS CLOCK1 53
121
121
BUS CLOCK2 54
123
123
128
DELAY LINE
OUTPUT 107
120
120
DELAY LINE
OUTPUT 108
128
122
122
129
INTERNAL
CLOCK 73
129
124
124
128
INTERNAL CLOCK
COMPLEMENT 74
126
126
128
INPUT
SAMPLE
127
125
127
125

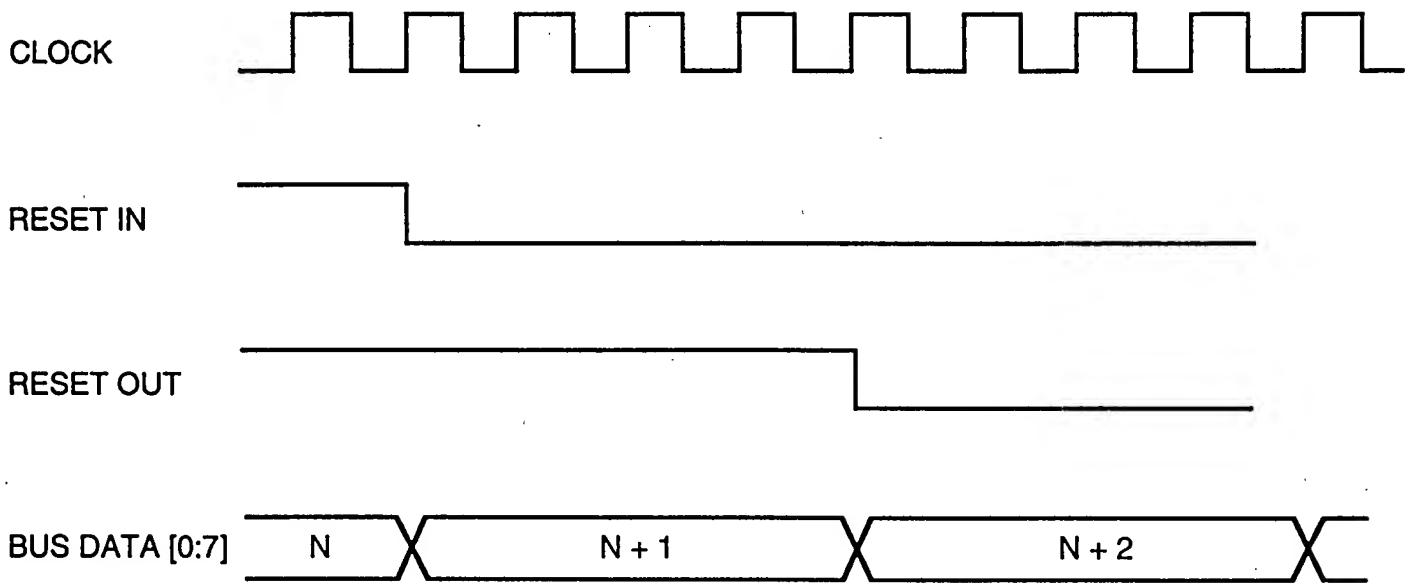
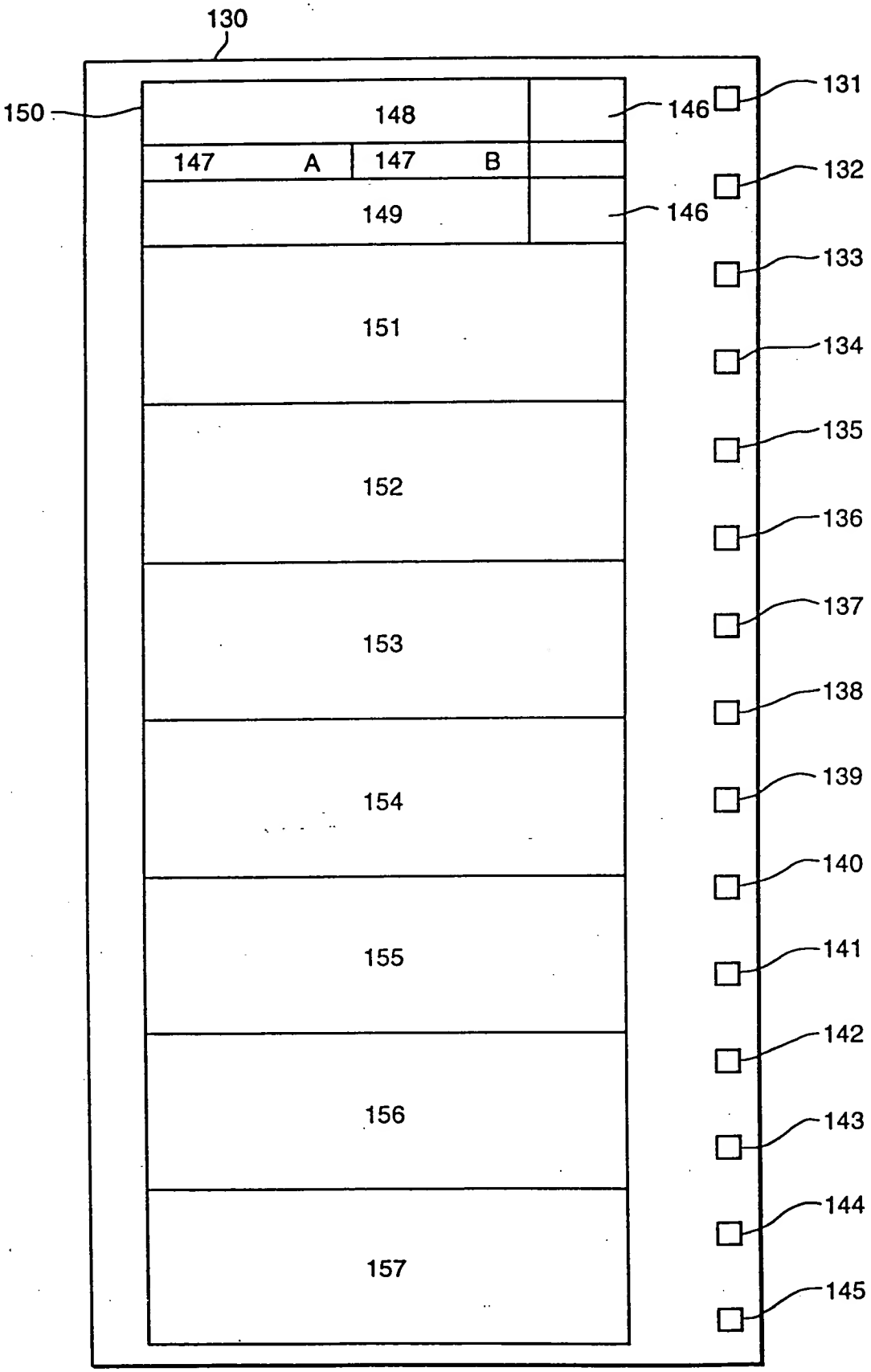


FIG_14

FIG_15


130
150
148
146
131
147
A
147
B
132
149
146
133
151
134
152
135
136
153
137
138
154
139
140
155
141
142
156
143
144
157
145